18Mb Pipelined QDR™II SRAM Burst of 2

IDT71P72804
IDT71P72604

Features

- 18Mb Density (1Mx18, 512kx36)
- Separate, Independent Read and Write Data Ports
  - Supports concurrent transactions
- Dual Echo Clock Output
- 2-Word Burst on all SRAM accesses
- DDR (Double Data Rate) Multiplexed Address Bus
  - One Read and One Write request per clock cycle
- DDR (Double Data Rate) Data Buses
  - Two word burst data per clock on each port
  - Four word transfers per clock cycle (2 word bursts on 2 ports)
- Depth expansion through Control Logic
- HSTL (1.5V) inputs that can be scaled to receive signals from 1.4V to 1.9V.
- Scalable output drivers
  - Can drive HSTL, 1.8V TTL or any voltage level from 1.4V to 1.9V.
  - Output Impedance adjustable from 35 ohms to 70 ohms
- Commercial and Industrial Temperature Ranges
- 1.8V Core Voltage (VDD)
- 165-ball, 1.0mm pitch, 13mm x 15mm fBGA Package
- JTAG Interface

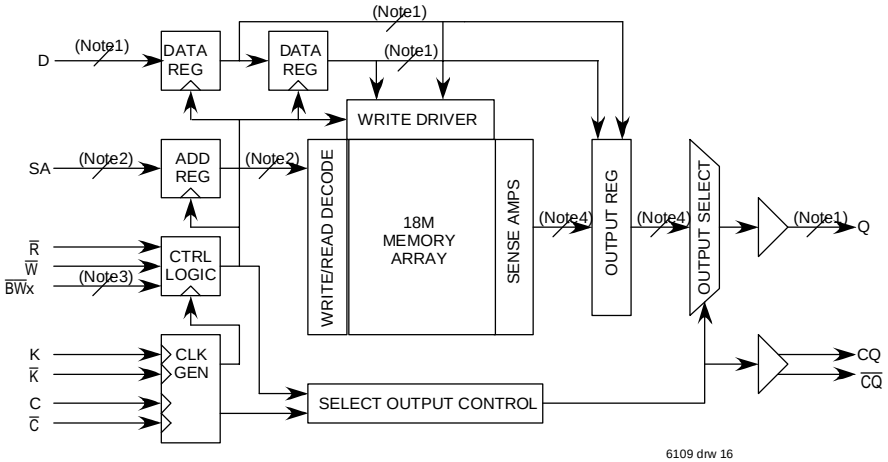
Description

The IDT QDRII™ Burst of two SRAMs are high-speed synchronous memories with independent, double-data-rate (DDR), read and write data ports. This scheme allows simultaneous read and write access for the maximum device throughput, with two data items passed with each read or write. Four data word transfers occur per clock cycle, providing quad-data-rate (QDR) performance. Comparing this with standard SRAM common I/O (CIO), single data rate (SDR) devices, a four to one increase in data access is achieved at equivalent clock speeds. Considering that QDRII allows clock speeds in excess of standard SRAM devices, the throughput can be increased well beyond four to one in most applications.

Using independent ports for read and write data access, simplifies system design by eliminating the need for bi-directional buses. All buses associated with the QDRII are unidirectional and can be optimized for signal integrity at very high bus speeds. The QDRII has scalable output impedance on its data output bus and echo clocks, allowing the user to tune the bus for low noise and high performance.

The QDRII has a single DDR address bus with multiplexed read and write addresses. All read addresses are received on the first half of the clock cycle and all write addresses are received on the second half of the clock cycle. The read and write enables are received on the first half of the clock cycle. The byte and nibble write signals are received on both halves of the clock cycle simultaneously with the data they are controlling on the data input bus.

Functional Block Diagram



Notes

1) Represents 18 signal lines for x18, and 36 signal lines for x36
2) Represents 19 address signal lines for x18, and 18 address signal lines for x36.
3) Represents 2 signal lines for x18, and 4r signal lines for x36.
4) Represents 36 signal lines for x18, and 72 signal lines for x36.

Absolute Maximum Ratings(1) (2)

Symbol	Rating	Value	Unit
V_{TERM}	Supply Voltage on V_{DD} with Respect to GND	–0.5 to +2.9	V
V_{TERM}	Supply Voltage on V_{DDQ} with Respect to GND	–0.5 to V_{DD} +0.3	V
V_{TERM}	Voltage on Input terminals with respect to GND.	–0.5 to V_{DD} +0.3	V
V_{TERM}	Voltage on Output and I/O terminals with respect to GND.	-0.5 to V_{DDQ} +0.3	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Continuous Current into Outputs	± 20	mA

6109 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDDQ must not exceed VDD during normal operation.

Write Descriptions(1,2,3)

Signal	$\overline{BW}_0$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$
Write Byte 0	L	X	X	X
Write Byte 1	X	L	X	X
Write Byte 2	X	X	L	X
Write Byte 3	X	X	X	L

6109 tbl 09

NOTES:
1) All byte write ($\overline{BW}$x) signals are sampled on the rising edge of K and again on $\overline{K}$. The data that is present on the data bus in the designated byte will be latched into the input if the corresponding $\overline{BW}$x is held low. The rising edge of K will sample the first byte of the two word burst and the rising edge of $\overline{K}$ will sample the second byte of the two word burst.
2) The availability of the $\overline{BW}$x on designated devices is described in the pin description table.
3) The QDRII Burst of two SRAM has data forwarding. A read request that is initiated on the same cycle as a write request to the same address will produce the newly written data in response to the read request.

Capacitance (TA = +25°C, f = 1.0MHz)(1)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{DD} = 1.8V, V_{DDQ} = 1.5V	5	pF
C_{CLK}	Clock Input Capacitance		6	pF
C_O	Output Capacitance		7	pF

6109 tbl 06

NOTE:
1. Tested at characterization and retested after any design or process change that may affect these parameters.

Recommended DC Operating and Temperature Conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		1.7	1.8	1.9	V
V_{DDQ}	I/O Supply Voltage		1.4	1.5	V_{DD}	V
V_{SS}	Ground		0	0	0	V
V_{REF}	Input Reference Voltage		0.68	V_{DDQ}/2	0.95	V
T_A	Ambient Temperature (1)	Commercial	0 to +70			°C
		Industrial	-40 to +85			°C

6109 tbl 04

NOTE:
1. During production testing, the case temperature equals the ambient temperature.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 1.8 ± 100mV, V_{DDQ} = 1.4V to 1.9V)

Parameter	Symbol	Test Conditions		Min	Max		Unit	Note
Input Leakage Current	I_{IL}	V_{DD} = Max V_{IN} = V_{SS} to V_{DDQ}		-2	+2		µA	
Output Leakage Current	I_{OL}	Output Disabled		-2	+2		µA	
					Com'l	Ind		
Operating Current (x36): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0mA (outputs open), Cycle Time ≥ t_{KHKH} Min	200MHz	-	950	1000	mA	1
			167MHz	-	850	900		
Operating Current (x18): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0mA (outputs open), Cycle Time ≥ t_{KHKH} Min	250MHz	-	850	-	mA	1,8
			200MHz	-	750	800		
			167MHz	-	650	700		
Standby Current: NOP	I_{SB1}	Device Deselected (in NOP state), Iout = 0mA (outputs open), f=Max, All Inputs ≤0.2V or ≥ VDD -0.2V	250MHz	-	375	-	mA	2,8
			200MHz	-	335	385		
			167MHz	-	300	350		
Output High Voltage	V_{OH1}	RQ = 250Ω, I_{OH} = -15mA		V_{DDQ}/2-0.12	V_{DDQ}/2+0.12		V	3,7
Output Low Voltage	V_{OL1}	RQ = 250Ω, I_{OL} = 15mA		V_{DDQ}/2-0.12	V_{DDQ}/2+0.12		V	4,7
Output High Voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DDQ}-0.2	V_{DDQ}		V	5
Output Low Voltage	V_{OL2}	I_{OL} = 0.1mA		V_{SS}	0.2		V	6

6109 tbl 10c

NOTES:

1. Operating Current is measured at 100% bus utilization.
2. Standby Current is only after all pending read and write burst operations are completed.
3. Outputs are impedance-controlled. IOH = -(VDDQ/2)/(RQ/5) and is guaranteed by device characterization for 175Ω≤ RQ < 350Ω. This parameter is tested at RQ = 250Ω, which gives a nominal 50Ω output impedance.
4. Outputs are impedance-controlled. IOL = (VDDQ/2)/(RQ/5) and is guaranteed by device characterization for 175Ω≤ RQ < 350Ω. This parameter is tested at RQ = 250Ω, which gives a nominal 50Ω output impedance.
5. This measurement is taken to ensure that the output has the capability of pulling to the VDDQ rail, and is not intended to be used as an impedance measurement point.
6. This measurement is taken to ensure that the output has the capability of pulling to Vss, and is not intended to be used as an impedance measurement point.
7. Programmable Impedance Mode.
8. Industrial temperature range is not available for the 250MHz speed grade.

Input Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

(V_{DD} = 1.8 ± 100mV, V_{DDQ} = 1.4V to 1.9V)

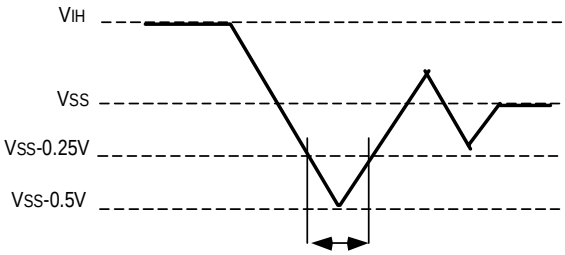
Parameter	Symbol	Min	Max	Unit	Notes
Input High Voltage, DC	V_{IH} (DC)	V_{REF} +0.1	V_{DDQ} +0.3	V	1,2
Input Low Voltage, DC	V_{IL} (DC)	-0.3	V_{REF} -0.1	V	1,3
Input High Voltage, AC	V_{IH} (AC)	V_{REF} +0.2	-	V	4,5
Input Low Voltage, AC	V_{IL} (AC)	-	V_{REF} -0.2	V	4,5

6109 tbl 10d

NOTES:

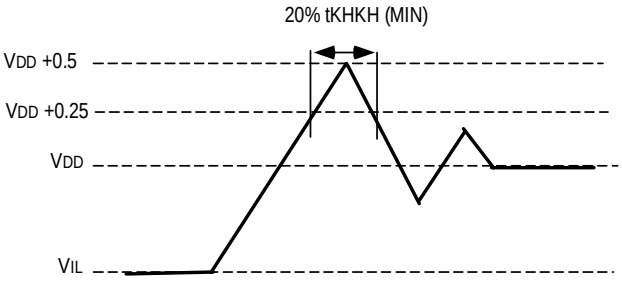
1. These are DC test criteria. DC design criteria is VREF ± 50mV. The AC VIH/VIL levels are defined separately for measuring timing parameters.
2. VIH (Max) DC = VDDQ+0.3, VIH (Max) AC = VDD +0.5V (pulse width ≤20% tKHKH (min))
3. VIL (Min) DC = -0.3V, VIL (Min) AC = -0.5V (pulse width ≤20% tKHKH (min))
4. This conditon is for AC function test only, not for AC parameter test.
5. To maintain a valid level, the transitioning edge of the input must:
   a) Sustain a constant slew rate from the current AC level through the target AC level, VIL(AC) or VIH(AC)
   b) Reach at least the target AC level.
   c) After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC)

Undershoot Timing



6109 drw 22

Overshoot Timing



6109 drw 21

AC Electrical Characteristics

(VDD = 1.8 ± 100mV, VDDQ = 1.4V to 1.9V, Commercial and Industrial Temperature Ranges) [3,7]

Symbol	Parameter	250MHz[10,11]		200MHz		167MHz		Unit	Notes
		Min.	Max	Min.	Max	Min.	Max		
Clock Parameters									
tKHKH	Clock Cycle Time (K,$\overline{K}$,C,$\overline{C}$)	4.00	6.30	5.00	7.88	6.00	8.40	ns	
tKC var	Clock Phase Jitter (K,$\overline{K}$,C,$\overline{C}$)	-	0.20	-	0.20	-	0.20	ns	1,5
tKHKL	Clock High Time (K,$\overline{K}$,C,$\overline{C}$)	1.60	-	2.00	-	2.40	-	ns	8
tKLKH	Clock LOW Time (K,$\overline{K}$,C,$\overline{C}$)	1.60	-	2.00	-	2.40	-	ns	8
tKH$\overline{K}$H	Clock to $\overline{clock}$ (K→$\overline{K}$,C→$\overline{C}$)	1.80	-	2.20	-	2.70	-	ns	9
t$\overline{K}$HKH	$\overline{Clock}$ to clock ($\overline{K}$→K,$\overline{C}$→C)	1.80	-	2.20	-	2.70	-	ns	9
tKHCH	Clock to data clock (K→C,$\overline{K}$→$\overline{C}$)	0.00	1.80	0.00	2.30	0.00	2.80	ns	
tKC lock	DLL lock time (K, C)	1024	-	1024	-	1024	-	cycles	2
tKC reset	K static to DLL reset	30	-	30	-	30	-	ns	
Output Parameters									
tCHQV	C,$\overline{C}$ HIGH to output valid	-	0.45	-	0.45	-	0.50	ns	3
tCHQX	C,$\overline{C}$ HIGH to output hold	-0.45	-	-0.45	-	-0.50	-	ns	3
tCHCQV	C,$\overline{C}$ HIGH to echo clock valid	-	0.45	-	0.45	-	0.50	ns	3
tCHCQX	C,$\overline{C}$ HIGH to echo clock hold	-0.45	-	-0.45	-	-0.50	-	ns	3
tCQHQV	CQ,$\overline{CQ}$ HIGH to output valid	-	0.30	-	0.35	-	0.40	ns	
tCQHQX	CQ,$\overline{CQ}$ HIGH to output hold	-0.30	-	-0.35	-	-0.40	-	ns	
tCHQZ	$\overline{C}$ HIGH to output High-Z	-	0.45	-	0.45	-	0.50	ns	3,4,5
tCHQX1	$\overline{C}$ HIGH to output Low-Z	-0.45	-	-0.45	-	-0.50	-	ns	3,4,5
Set-Up Times									
tAVKH	Address valid to K,$\overline{K}$ rising edge	0.35	-	0.40	-	0.50	-	ns	6
tIVKH	$\overline{R}$, $\overline{W}$ inputs valid to K,$\overline{K}$ rising edge	0.35	-	0.40	-	0.50	-	ns	
tDVKH	Data-in and $\overline{BWx}$ valid to K, $\overline{K}$ rising edge	0.35	-	0.40	-	0.50	-	ns	
Hold Times									
tKHAX	K,$\overline{K}$ rising edge to address hold	0.35	-	0.40	-	0.50	-	ns	6
tKHIX	K,$\overline{K}$ rising edge to $\overline{R}$, $\overline{W}$ inputs hold	0.35	-	0.40	-	0.50	-	ns	
tKHDX	K, $\overline{K}$ rising edge to data-in and $\overline{BWx}$ hold	0.35	-	0.40	-	0.50	-	ns	

6109 tbl 11

NOTES:

1. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
2. Vdd slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once Vdd and input clock are stable.
3. If C,$\overline{C}$ are tied High, K,$\overline{K}$ become the references for C,$\overline{C}$ timing parameters.
4. To avoid bus contention, at a given voltage and temperature tCHQX1 is bigger than tCHQZ.
   The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worse case at totally different test conditions (0°C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7V)
   It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
5. This parameter is guaranteed by device characterization, but not production tested.
6. All address inputs must meet the specified setup and hold times for all latching clock edges.
7. During production testing, the case temperature equals TA.
8. Clock High Time (tKHKL) and Clock Low Time (tKLKH) should be within 40% to 60% of the cycle time (tKHKH).
9. Clock to Clock time (tKH$\overline{K}$H) and Clock to Clock time (t$\overline{K}$HKH) should be within 45% to 55% of the cycle time (tKHKH).
10. The 250MHz speed grade is not available in the 512K x 36-bit option.
11. Industrial temperature range is not available for the 250MHz speed grade.

JTAG DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
I/O Power Supply	V_{DDQ}	1.4	-	V_{DD}	V	
Power Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Input High Level	V_{IH}	1.3	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.5	V	
TCK Input Leakage Current	I_{IL}	-5	-	+5	µA	
TMS, TDI Input Leakage Current	I_{IL}	-15	-	+15	µA	
TDO Output Leakage Current	I_{0L}	-5	-	+5	µA	
Output High Voltage (I_{OH} = -1mA)	V_{OH}	V_{DDQ} - 0.2	-	V_{DDQ}	V	1
Output Low Voltage (I_{OL} = 1mA)	V_{OL}	V_{SS}	-	0.2	V	1

6109 tbl 19

NOTE:

1. The output impedance of TDO is set to 50 ohms (nominal process) and does not vary with the external resistor connected to ZQ.

JTAG AC Test Conditions

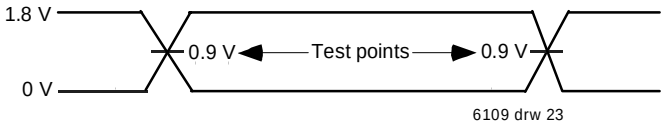
Parameter	Symbol	Value	Unit	Note
Input High Level	V_{IH}	1.8	V	
Input Low Level	V_{IL}	0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	1

6109 tbl 20

NOTE:

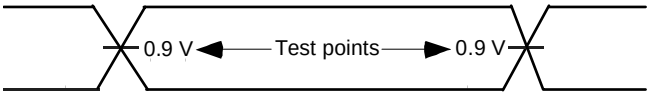
1. For SRAM outputs see AC test load on page 11.

JTAG Input Test WaveForm



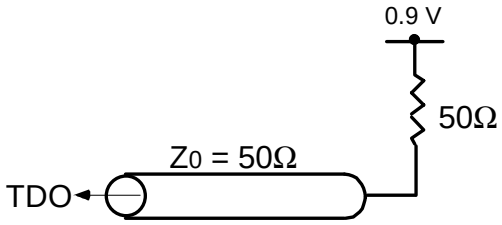
6109 drw 23

JTAG Output Test WaveForm



6109 drw 23a

JTAG AC Test Load



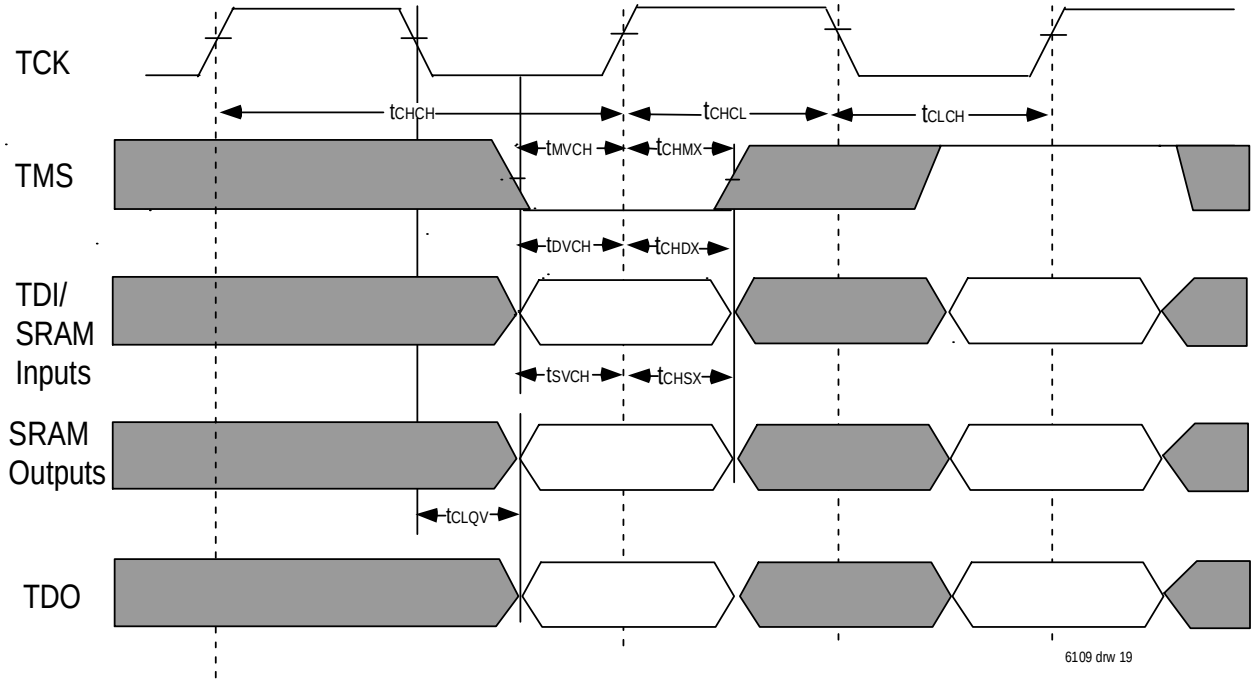
6109 drw 24

JTAG AC Characteristics

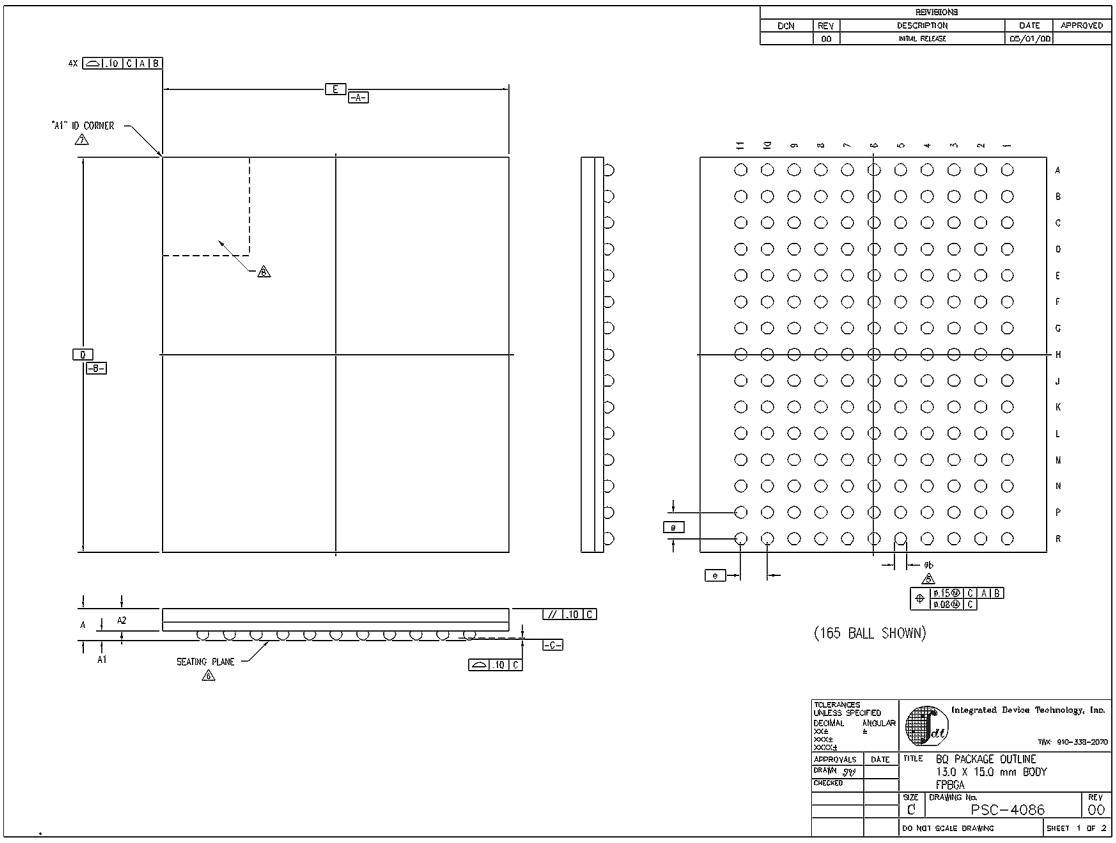
Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

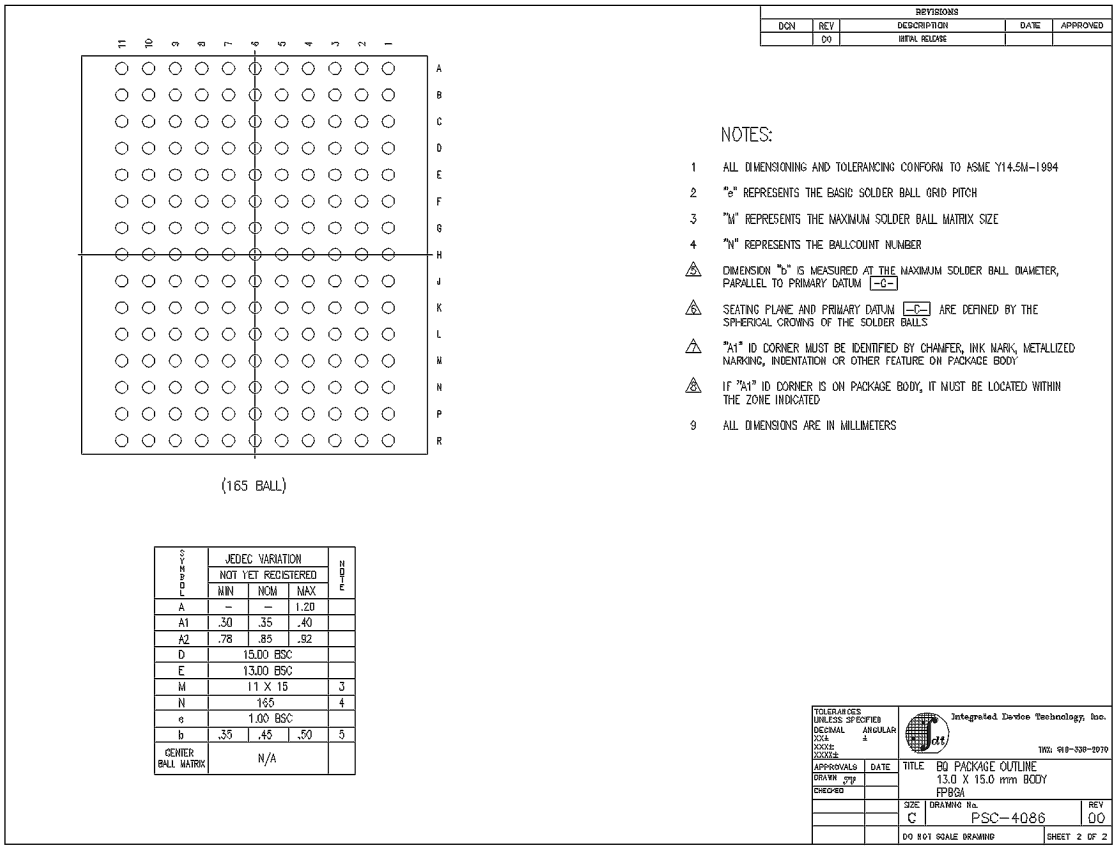
6109 tbl.21

JTAG Timing Diagram

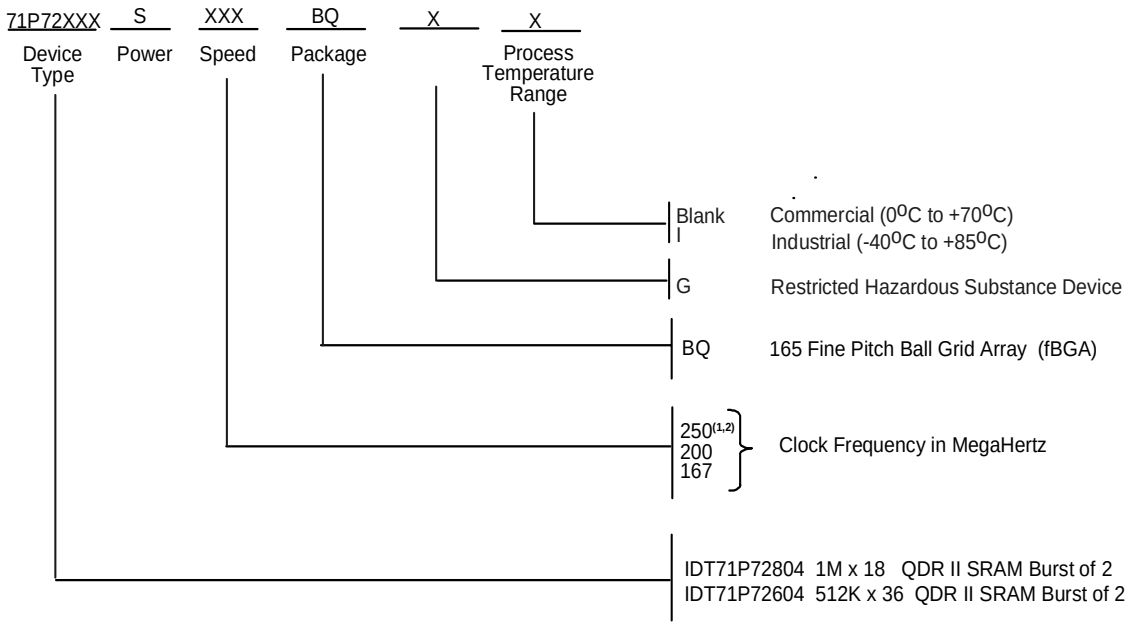


Package Diagram Outline for 165-Ball Fine Pitch Grid Array





Ordering Information



Notes:

6109 drw 15

1) The 250MHz speed grade is not available in the 512K x36-bit option.

2) Industrial temperature range is not available for the 250MHz speed grade.